

FIG. 1(Prior Art)

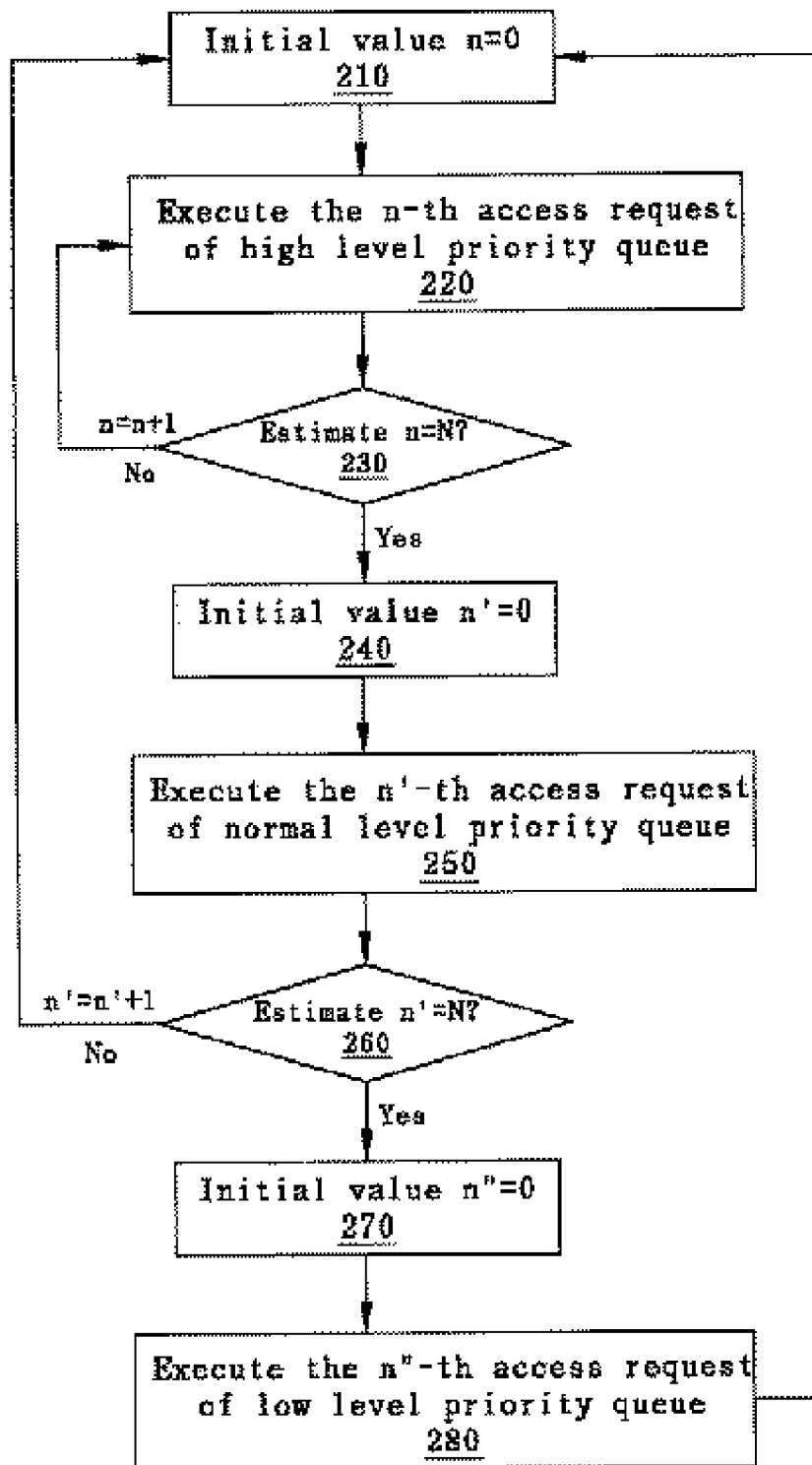


FIG. 2

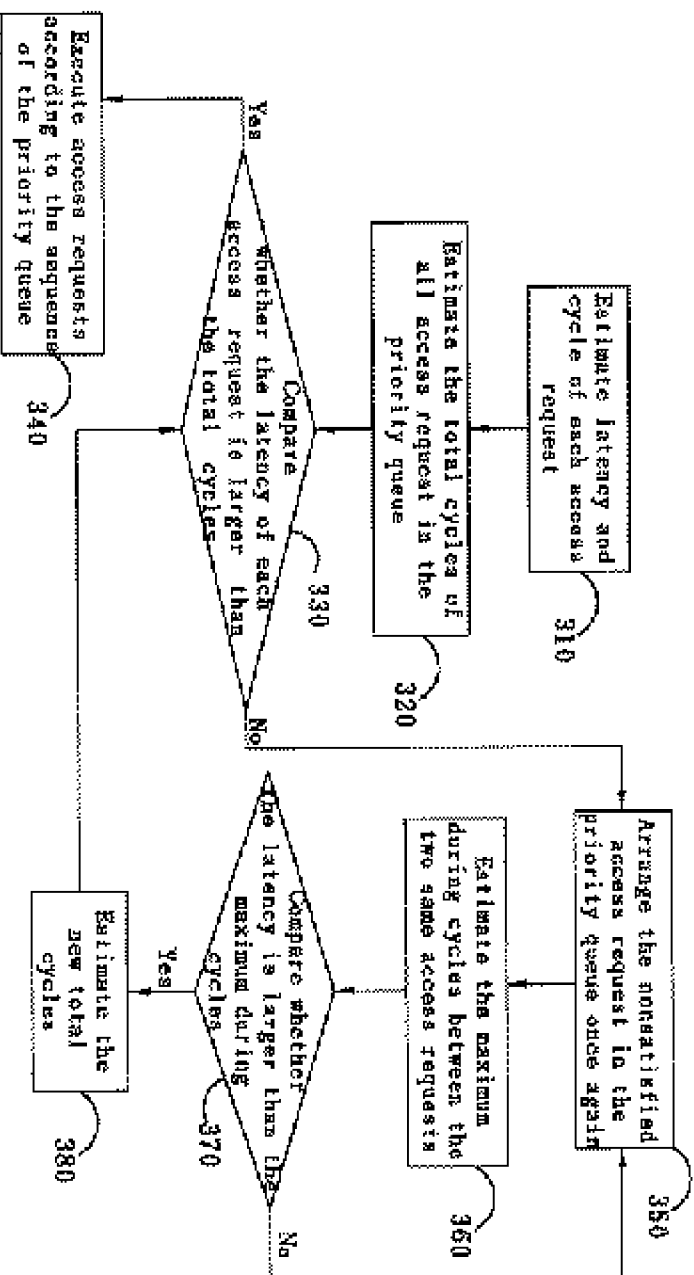


FIG. 3

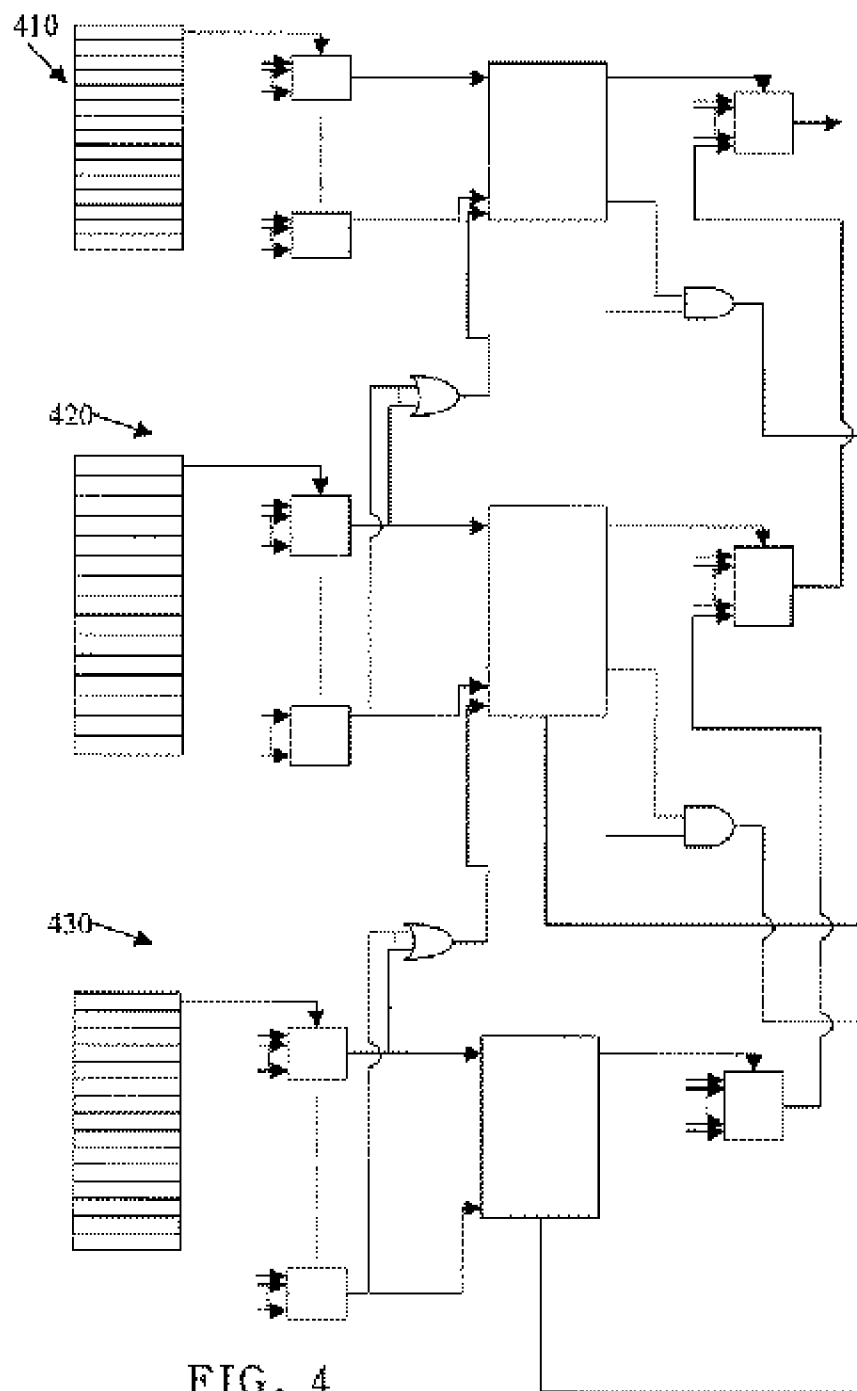


FIG. 4

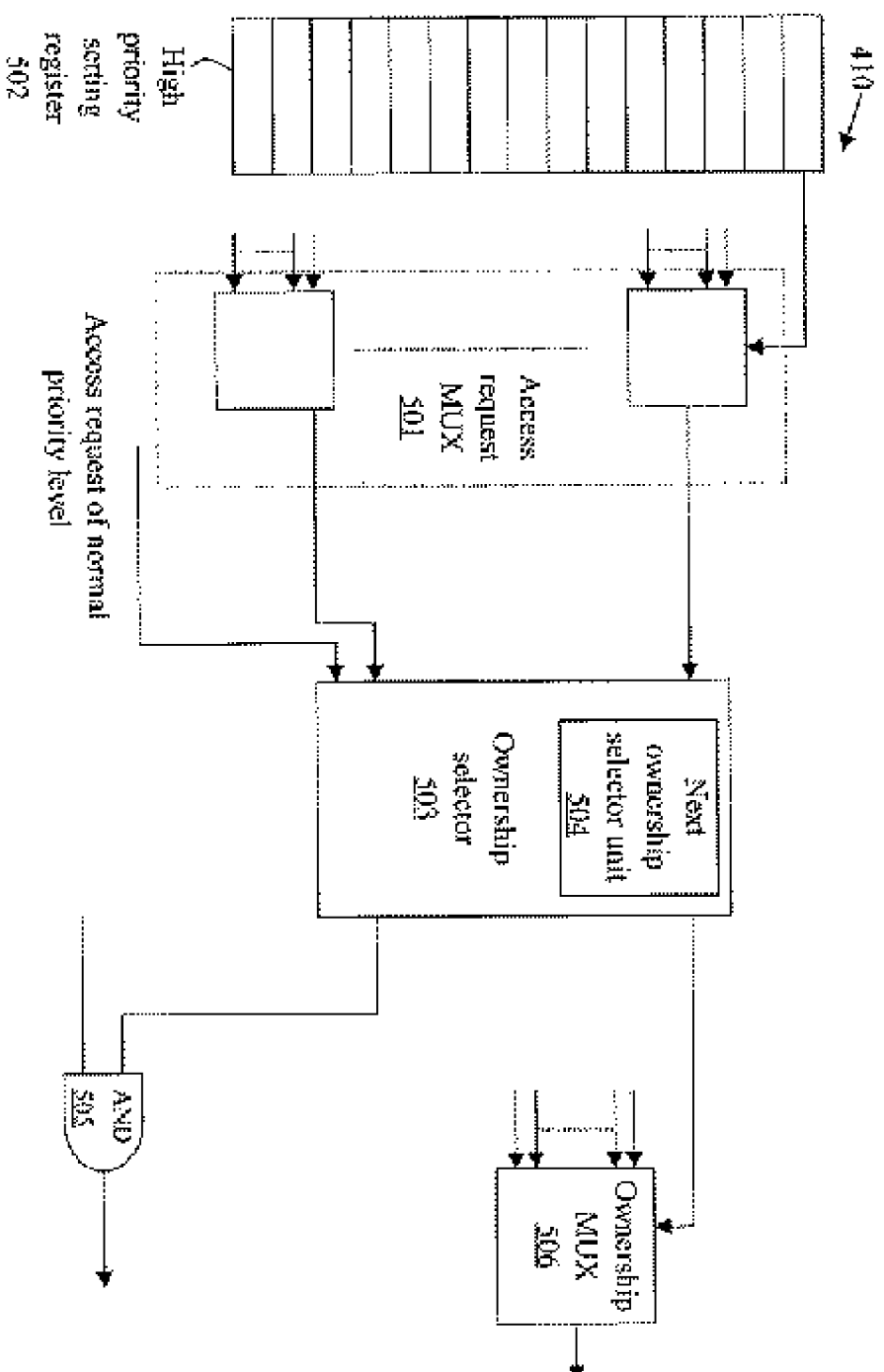


FIG. 5

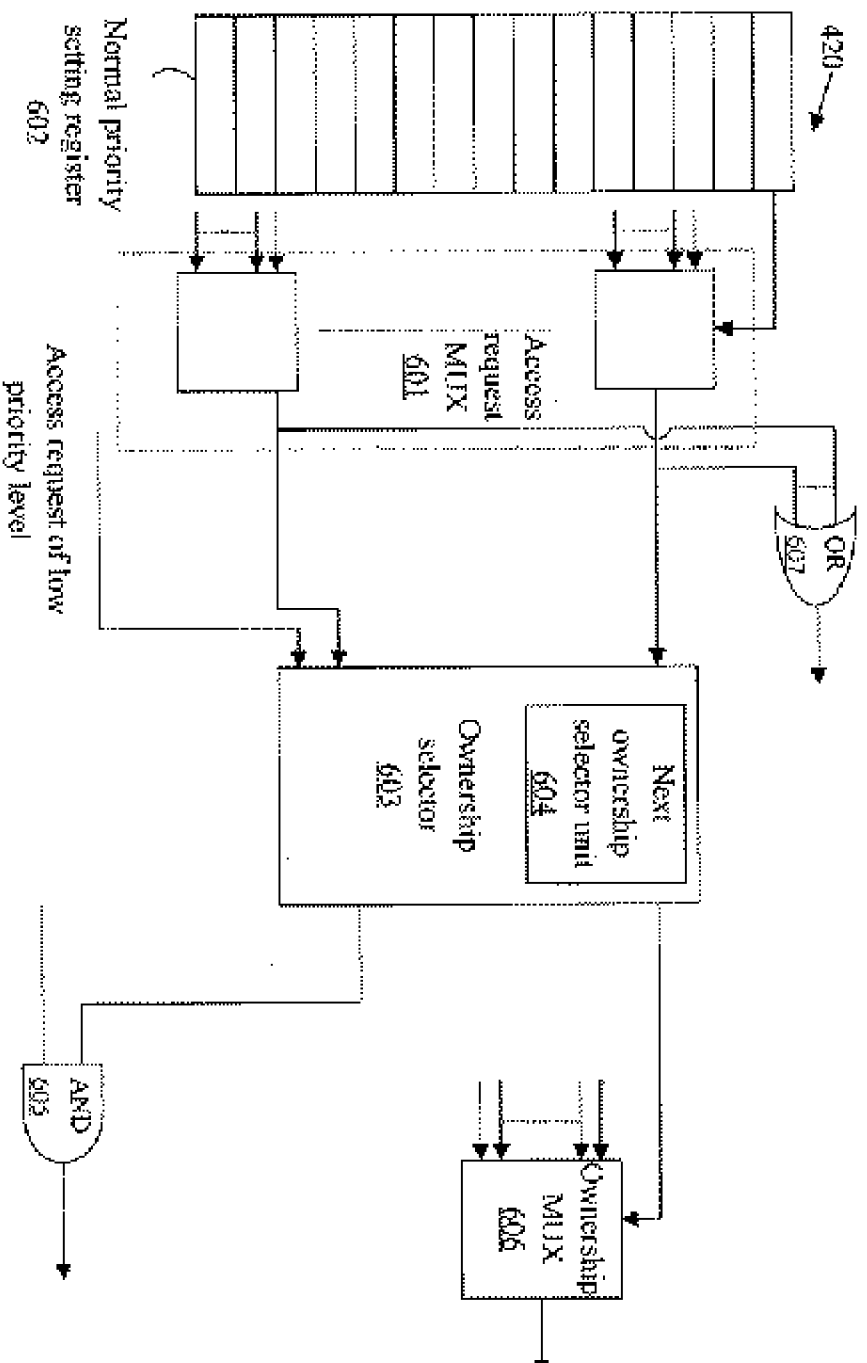


FIG. 6

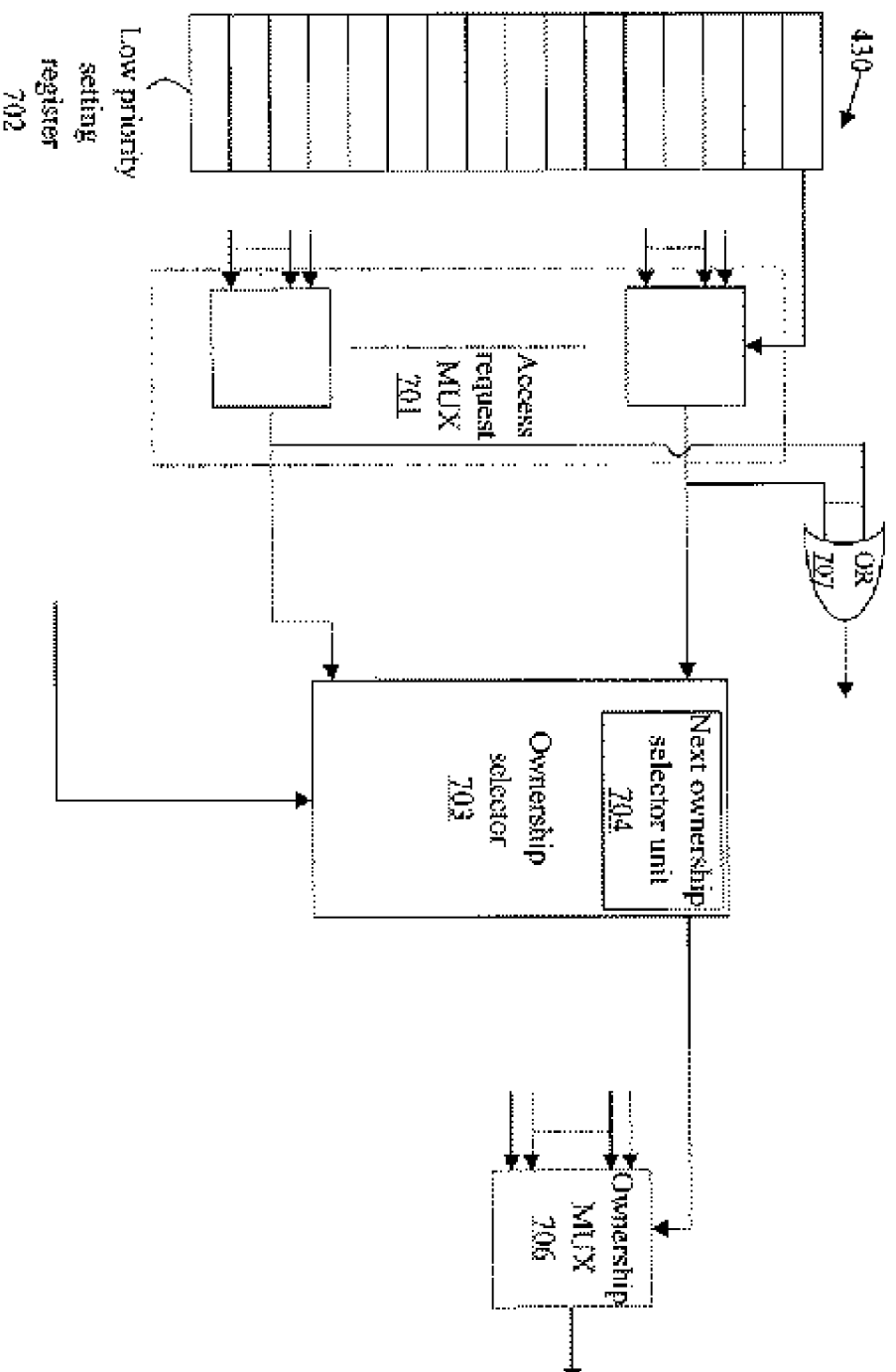


FIG. 7

| Seq | NO | Burst Length | Cycle(T) | Latency(T) |
|-----|----|--------------|----------|------------|
| H6 | 3 | 64 | 36 | 128 |
| H11 | 19 | 24 | 10 | 111 |
| H21 | 10 | 12 | 5 | 76 |
| H31 | 23 | 32 | 12 | 149 |
| H41 | 11 | 16 | 6 | 120 |
| H5 | | | 0 | |
| H6 | | | 0 | |
| H7 | | | 0 | |
| H8 | | | 0 | |
| H9 | | | 0 | |
| H10 | | | 0 | |
| H11 | | | 0 | |
| H12 | | | 0 | |
| H13 | | | 0 | |
| H14 | | | 0 | |
| H15 | N | 48 | 20 | |

High Priority

| Seq | NO | Burst Length | Cycle(T) | Latency(T) |
|-----|----|--------------|----------|------------|
| N6 | 23 | 8 | 3 | 930 |
| N1 | 21 | 32 | 13 | 261 |
| N2 | 6 | 32 | 13 | 660 |
| N1 | 22 | 32 | 13 | 606 |
| N4 | | | 0 | |
| N1 | | | 0 | |
| N6 | | | 0 | |
| N7 | | | 0 | |
| N8 | | | 0 | |
| N9 | | | 0 | |
| N10 | | | 0 | |
| N11 | | | 0 | |
| N12 | | | 0 | |
| N13 | | | 0 | |
| N14 | | | 0 | |
| N15 | L | 48 | 20 | |

Normal Priority

| Seq | NO | Burst Length | Cycle(T) | Latency(T) |
|-----|----|--------------|----------|------------|
| L0 | 2 | 32 | 13 | 3621 |
| L1 | 5 | 32 | 10 | 4250 |
| L2 | 8 | 32 | 13 | Infinite |
| L3 | 19 | 32 | 13 | 3320 |
| L4 | 34 | 32 | 13 | Infinite |
| L5 | | | 0 | |
| L6 | | | 0 | |
| L7 | | | 0 | |
| L8 | | | 0 | |
| L9 | | | 0 | |
| L10 | | | 0 | |
| L11 | | | 0 | |
| L12 | | | 0 | |
| L13 | | | 0 | |
| L14 | | | 0 | |
| L15 | | | 0 | |

Low Priority

Total cycles : 80

62: 5 300 362

72: 5 1400 1472

FIG. 8

High Priority

| REQ NO. | Burst Length | Cycle(T) | Latency(T) |
|---------|--------------|----------|------------|
| H0 | 3 | 64 | 26 |
| H1 | 19 | 24 | 10 |
| H2 | 10 | 12 | 5 |
| H3 | 23 | 32 | 13 |
| H4 | 11 | 16 | 6 |
| H5 | 10 | 12 | 5 |
| H6 | | | 0 |
| H7 | | | 0 |
| H8 | | | 0 |
| H9 | | | 0 |
| H10 | | | 0 |
| H11 | | | 0 |
| H12 | | | 0 |
| H13 | | | 0 |
| H14 | | | 0 |
| H15 | N | 48 | 20 |

Normal Priority

| REQ NO. | Burst Length | Cycle(T) | Latency(T) |
|---------|--------------|----------|------------|
| N0 | 25 | 8 | 1 |
| N1 | 21 | 32 | 13 |
| N2 | 6 | 32 | 13 |
| N3 | 22 | 32 | 13 |
| N4 | 21 | 32 | 13 |
| N5 | | | 0 |
| N6 | | | 0 |
| N7 | | | 0 |
| N8 | | | 0 |
| N9 | | | 0 |
| N10 | | | 0 |
| N11 | | | 0 |
| N12 | | | 0 |
| N13 | | | 0 |
| N14 | | | 0 |
| N15 | L | 48 | 20 |

Low Priority

| REQ NO. | Burst Length | Cycle(T) | Latency(T) |
|---------|--------------|----------|------------|
| L0 | 2 | 32 | 13 |
| L1 | 5 | 48 | 20 |
| L2 | 8 | 32 | 13 |
| L3 | 18 | 32 | 13 |
| L4 | 24 | 32 | 13 |
| L5 | | | 0 |
| L6 | | | 0 |
| L7 | | | 0 |
| L8 | | | 0 |
| L9 | | | 0 |
| L10 | | | 0 |
| L11 | | | 0 |
| L12 | | | 0 |
| L13 | | | 0 |
| L14 | | | 0 |
| L15 | | | 0 |

Total cycles : 85

62
5 100
365

72
5 1400
1472

FIG. 9